REMARKS

Claims 1-25 are pending. Claims 1-4 and 12-14 are presently cancelled. Claims 10 and 11 have been previously allowed. Claim 7 has been rewritten in independent form, and claim 16 has been amended to include the limitations of base claim 15. Applicant requests reconsideration of the application in light of the following remarks.

Rejections under 35 U.S.C. § 102

Claims 21, 23, and 24 stand rejected under 35 U.S.C. § 102(b) in light of U.S. Patent No. 6,504,192 to Hasunuma ("Hasunuma"). As the PTO provides in MPEP § 2131, "[t]o anticipate a claim, the reference must teach every element of the claim...." (emphasis added). Therefore, each reference applied under 35 U.S.C. § 102 must disclose all of the elements of the claims to sustain the rejection. Accordingly, Applicant respectfully traverses the rejections on the following grounds.

Claim 21

Claim 21 reads:

> A transistor structure, comprising: (a) a semiconductor substrate having isolation regions and a plurality of transistor regions including first, second, and third transistor regions comprised of a dielectric layer formed on said substrate between said isolation regions; (b) a gate electrode having a first thickness formed on said dielectric layer in said first transistor region, a gate electrode having a second thickness formed on said dielectric layer in said second transistor region, and a gate electrode having a third thickness formed on said dielectric layer in said third transistor region; (c) oxide spacers having a first width formed adjacent to said gate electrode in the first transistor region, oxide spacers having a second width that is less than said first width formed adjacent to said gate electrode in the second transistor region, and oxide spacers having a third width less than said second width formed adjacent to said gate electrode in the third transistor region.

Hasunuma does not teach every element of claim 21. For instance, claim 21 teaches a plurality of transistor regions formed "between" isolation regions. Hasunuma in Fig. 5 as referenced by the examiner shows only one isolation region (11), and the transistor regions

(designated in Hasunuma as B, A, C) are thus not located "between" regions. Additionally, Hasunuma does not teach oxide spacers of three widths as claim 21 does. Specifically, Hasunuma teaches two different widths in Fig. 6, spacer 3b having a greater width than spacer 3a (see col. 4 line 61-63). Contrary to the examiner's position, Hasunuma does not teach a third spacer width, 3c (Hasunuma Fig. 5). Also additionally, Hasunuma's method of teaching the control of spacer width is through the placement of dummy electrode adjacent to and a determined distance away from the transistor spacer sought to be controlled. This arrangement by necessity gives a transistor B with spacer thickness 3b in Fig. 6 greater than the spacer of transistor B nearer transistor A. The spacers in claim 21 however are uniform for a given transistor, as they are of a "first width" for a "first transistor." Therefore, for these mutually exclusive reasons, the rejection is not supported by the Hasunuma reference and should be withdrawn.

Claims 23 and 24

Claims 23 and 24 depend from and further limit Claim 21 and are allowable for at least the same reasons as claim 21.

Additionally and independently, claim 24 states that the "width of said oxide spacers is between about 10 and 1000 Angstroms." Hasunuma does not teach the width of oxide spacers as stated by the office action, but teaches only a film thickness of silicon dioxide of 100 to 5000 Angstroms prior to the formation of the spacers by etch processing of that silicon dioxide layer. (col. 4 line 47-50: "The silicon dioxide film 3 is an insulating film...and has a film thickness of 10 to 500 nm.") Therefore, Hasunuma does not teach all the elements of claim 24 and the rejection should be withdrawn for at least this reason.

Rejections under 35 U.S.C. § 103

Claims 5, 6, 10, 11, 15, 18-22, 24, and 25 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over 5,021,354 to Pfiester ("Pfiester") in view of 5,874,330 to Ahn ("Ahn"). Under MPEP § 2142, "[i]f the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness." Applicant respectfully traverses these rejections as it is submitted that the office action fails to factually support a prima facie case of obviousness based on the cited references for the following mutually exclusive reasons.

Independent Claims: 5, 21, 15

A. Combination of References fails to teach or suggest all claim limitations.

As provided in MPEP § 2143, "[t]o establish a prima facie case of obviousness,... the prior art reference (or references when combined) must teach or suggest all the claim limitations. The Applicant respectfully submits that the rejections of the following independent claims should be withdrawn at least because they do not meet this requirement.

Claim 5: Claim 5 reads in part:

> (c) forming an oxide layer on the substrate and on the gate electrodes in said plurality of transistor regions; and (d) etching said oxide layer to form spacers with a first width adjacent to said first gate electrode, spacers having a second width less than said first width adjacent to said second gate electrode, and spacers having a third width less than said second width adjacent to said third gate electrode.

Thus, claim 5 discloses three different oxide spacer widths. As stated by the examiner, Pfiester discloses only two different spacer widths and fails to disclose any additional widths. The Applicant respectfully submits that Ahn fails to cure this deficiency. Ahn discloses a manner of making different spacer widths on the transistors of the peripheral circuit region as opposed to the transistors of the cell region of the circuit. However, Ahn accomplishes this difference in spacer widths by using nitride spacers for the transistors of the cell region and in a separate process step forming oxide spacers for the transistors of the peripheral circuit. (col. 3 line 37-56, Fig. 2d, 2e).

This creates oxide spacers of a first width, and nitride spacers of a second width. Because claim 5 discloses a method including oxide spacers on each of the three transistors with varying spacer widths, all the elements of the claim are not met by this prior art combination as third oxide spacer width is not taught. Additionally, claim 5 discloses forming an oxide layer, and etching said layer to form spacers. Therefore, Ahn's requirement of depositing two films (one oxide and one nitride) to create spacers (rather than the one film in claim 5) does not meet all the elements of claim 5. Thus, claim 5 is allowable for at least this reason.

Claim 21 : Claim 21, for a transistor structure, reads in part:

> (c) oxide spacers having a first width formed adjacent to said gate electrode in the first transistor region, oxide spacers having a second width that is less than said first width formed adjacent to said gate electrode in the second transistor region, and oxide spacers having a third width less than said second width formed adjacent to said gate electrode in the third transistor region.

Thus, claim 21 discloses a device with three different oxide spacer widths. As stated by the examiner, Pfiester discloses only two different spacer widths and fails to disclose any additional widths. The Applicant respectfully submits that Ahn fails to cure this deficiency. Ahn discloses a manner of making different spacer widths on the transistors of the peripheral circuit as opposed to the transistors of the cell region. However, Ahn accomplishes this by using a nitride spacer for the transistors of the cell region and oxide spacer for the transistors of the peripheral circuit. (col. 3 line 37-56, Fig. 2d, 2e). This creates oxide spacers of one width, and nitride spacers of another width. Because claim 21 discloses a structure including spacers made from oxide on each of the three transistors with varying spacer widths, all the elements of the claim are not met by this prior art combination.

Claim 15: Claim 15, for a transistor structure, reads in part:

> (c) oxide spacers having a width formed adjacent to said gate electrodes in said first, second, and third transistor regions; and (d) silicon nitride spacers having a first width formed on said oxide spacers in said first transistor region, silicon

> nitride spacers having a second width less than said first width formed on said oxide spacers in said second transistor region, and silicon nitride spacers having a third width less than said second width formed on said oxide spacers in said third transistor region.

The Applicant respectfully submits that all elements of the claim are not met and therefore the rejection should be withdrawn for at least this reason. For instance, claim 15 discloses a structure where oxide spacers are adjacent to the gate electrodes; and silicon nitride spacers with varying widths are on said oxide spacers. Pfiester does not teach using spacers of two different materials (oxide and silicon nitride) on the same transistor. Ahn fails to cure this deficiency as it teaches using nitride on the cell region and oxide on the peripheral circuit for each region's spacers, but does not teach any combination of the two materials for one transistor. Additionally, Pfiester, as stated by the office action, teaches only two spacer widths. The applicant submits that Ahn fails to cure this deficiency. Ahn teaches two different spacer widths by using one material, oxide, for one set of transistors and a separate layer, nitride, for another set of transistors. In the Ahn disclosure, this gives oxide spacer of one width, and nitride spacer of a second width on separate transistors. Because claim 15 uses the same structure for spacer materials for the three transistors with varying spacer widths (oxide spacers with silicon nitride spacers of varying widths on said oxide spacers), all the elements of claim 15 are not met by the combination these two references and the rejections should be withdrawn for at least this reason.

B. References that teach away from claimed invention cannot be used to establish obviousness

MPEP § 2142.02 requires that "[a] prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention."

Claim 5: The Applicant submits that, additionally and independently to the above, because Ahn teaches away from the claimed invention the rejection should be withdrawn. Ahn teaches developing different spacer widths as a consequence of using two different materials, oxide and nitride for the spacers depending on the location of the transistor on the device circuitry (oxide on

the peripheral circuit having one width and nitride on the cell region having a second width). Thus, the Ahn disclosure teaches away from using a single layer to create various spacer widths. The claimed invention in claim 5 is creating spacers of different widths using oxide in a single layer, not requiring separate layers or materials.

Claim 21: Ahn teaches the development of different spacer widths through using two different materials, oxide for one set of transistors and nitride for another set of transistors depending on the location on the device with the oxide spacers being of one width and the nitride spacers being of a second width. Therefore, by requiring two separate materials/layers, the Applicant submits that the Ahn disclosure teaches away from using a single material to create spacers of different widths. Claim 21 has spacers of various widths consisting of a single material: oxide.

Claim 15: Ahn teaches the development of different spacer widths through using two different materials, oxide for one set of transistors and nitride for another set of transistors depending on the location on the device of the transistors, with the oxide spacers being of one width and the nitride spacers being of a second width. Therefore, by requiring different materials/layers for the spacers that are to be of different widths, the Applicant submits that the Ahn disclosure teaches away from using the same materials on various transistors to create spacers of different widths. Claim 15 discloses an oxide spacer with a silicon nitride spacer on said oxide spacer for each of the transistors with varying spacer width.

Additionally and independently, Ahn teaches away from using nitride on the peripheral cell region. Ahn states "However, the use of an identical nitride in the formation of spacer for an element in a cell region as well as for an element in the peripheral circuit has caused problems as follows. First, the use of nitride in the formation of sidewalls for an element in a peripheral circuit increases an overlap capacitance of the gate-source electrodes, and causes an adverse effect on the device due to an increase in hot carrier generation." (Col. 1 lines 41-50). Therefore, Ahn teaches away from the Claim 15 which uses nitride on the gate electrode spacers of different widths.

C. There is no motivation to combine these references

Claims 5, 21, 15

Furthermore, even if Pfiester and Ahn were properly combinable (which they clearly are not, as previously described), the case law is clear that there must be evidence that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. It is also clear that a rejection cannot be predicated on the mere identification of individual components of claimed limitations. Rather, particular findings must be made as the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed. *Ecolochem Inc. v. Southern California Edison*, 56 USPQ 2d 1065, 1076 (Fed. Cir. 200) (emphasis added). Therefore, the Applicant respectfully submits that the examiner has not met his burden of supporting a prima facie case of obviousness and as such the rejections for independent claims 5, 15, and 21 should be withdrawn.

Dependant Claims: 6, 22, 24, 25, 18, 19, 20

The Applicant submits that the rejection of the following dependant claims should also be withdrawn for the following mutually exclusive reasons.

Claim 6: As claim 6 depends from and further limits claim 5 it is allowable for at least the same reasons as claim 5 (see above).

Claim 22: Claim 22 depends upon and further limits claim 21 and should be allowable for at least the same reasons as claim 22 (see above).

Claim 24: Claim 24 depends upon and further limits claim 21 and should be allowable for at least the same reasons as claim 21 (see above).

Additionally and independently the Applicant traverses the rejection as, per MPEP § 2143, "[t]o establish a prima facie case of obviousness,... the prior art reference (or references when combined) must teach or suggest all the claim limitations. Claim 24 states that the "width of said oxide spacers is between about 10 and 1000 Angstroms." Applicant submits that Pfiester does not teach this element as the office action states. Pfiester states: "A thin layer of oxide 28 or other insulating material is formed on the exposed surface of polycrystalline silicon layer 26. Preferably oxide layer 28 is a thermally grown oxide having a thickness of about 20 nanometers. Oxide layer 28 provides a screen oxide for a subsequent implantation and also serves to protect polycrystalline silicon 26 from contamination." (Col. 2 line 45-51). This oxide layer is not the oxide layer used to create the spacers in Pfiester. Specifically, Pfiester continues to disclose "the process continues by the deposition of a sidewall spacer forming material 52 overlaying the entire structure" and further continues "The spacer forming material such as polycrystalline silicon is deposited by chemical vapor deposition to a thickness of about 100-350 nanometers." (Col. 4 line 54-63). Even this teaching by Pfiester does not teach the width of the spacer; Pfiester teaches only for the thickness of the as deposited layer that will be used to create the spacers, not the spacer width. Ahn fails to cure this deficiency.

Claim 25: As Claim 25 depends from and further limits claim 21, it should be allowed for at least the same reasons as claim 21 (see above).

Claim 18: Claim 18 depends upon and further limits claim 15 and should be allowable for at least the same reasons as claim 15 (see above).

Additionally and independently, the Applicant traverses the rejection as, per MPEP § 2143, "[t]o establish a prima facie case of obviousness,... the prior art reference (or references when combined) must teach or suggest all the claim limitations. Claim 18 states that the "width of said oxide spacers is between about 10 and 1000 Angstroms." Applicant submits that Pfiester does not teach this element as the office action contends. Pfiester states: "A thin layer of oxide 28 or other

insulating material is formed on the exposed surface of polycrystalline silicon layer 26. Preferably oxide layer 28 is a thermally grown oxide having a thickness of about 20 nanometers. Oxide layer 28 provides a screen oxide for a subsequent implantation and also serves to protect polycrystalline silicon 26 from contamination." (Col. 2 line 45-51). This oxide layer is not the oxide layer used to create the spacers in Pfiester. Specifically, Pfiester continues to disclose "the process continues by the deposition of a sidewall spacer forming material 52 overlaying the entire structure" and further continues "[t]he spacer forming material such as polycrystalline silicon is deposited by chemical vapor deposition to a thickness of about 100-350 nanometers." (Col. 4 line 54-63). Even this teaching by Pfiester does not teach the width of the spacer; Pfiester teaches only for the thickness of the as deposited layer that will be used to create the spacers, not the spacer width itself. Ahn fails to cure this deficiency.

Claim 19: Claim 19 depends upon and further limits claim 15 and should be allowable for at least the same reasons as claim 15 (see above).

Additionally and independently, the Applicant traverses the rejection as, per MPEP § 2143, "[t]o establish a prima facie case of obviousness,... the prior art reference (or references when combined) must teach or suggest all the claim limitations. Claim 19 requires the silicon nitride spacer widths be between about 10 and 1000 Angstroms. The Applicant respectfully submits that Pfiester does not teach this element of the claim as alleged in the office action. Pfiester reads "[t]he spacer forming material, such as polycrystalline silicon is deposited by chemical vapor deposition to a thickness of about 100-350 nanometers." This is 1000 – 3500 Angstroms of deposited spacer forming material. This is not within the range disclosed by claim 19. Moreover, this is a measurement of the film material as deposited in Pfiester, and not a measurement of the width of the spacer as is stated in claim 19.

Claim 20: Claim 20 depends upon and further limits claim 15 and should be allowable for at least the same reasons as claim 15 (see above).

Conclusion

It is respectfully submitted that all the claims in the application are in condition for allowance. Should the Examiner deem that any further amendment is needed to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the below listed telephone number.

Respectfully submitted,

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